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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/918,600	07/30/2001	Ping-Sheng Tseng	16503-302501	8219

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EXAMINER	
SAXENA, AKASH	
ART UNIT	**PAPER NUMBER**
2128	

DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/918,600	TSENG ET AL.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-37 have been presented for examination based on the application filed on 30th July 2001.
2. Acknowledgement is made of change in power of attorney to "Moser, Patterson & Sheridan LLP" and change of correspondence of address filed on 4th April 2005.

Priority

3. This application appears to be continuation in part (CIP) of applications 09900124, which claims priority from 09373014, which claims priority from 09144222 making the effective filing date of the current application 31st August 1998.

Specification

4. The abstract of the disclosure is objected to because title of the abstract does not match the title in the specification. Correction is required. See MPEP § 608.01(b).
5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

6. Claims 4, 8, 18, 22, 31 are objected to due to improper numbering.

A series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim.

A claim, which depends from a dependent claim, should not be separated by any claim, which does not also depend from said dependent claim. It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n).

7. Claim 29 is objected to as it discloses "test bench process" servicing the signal. The objection is raised because the previous claim 28 discloses "host workstation" servicing the signal and as understood the phrases "test bench process" and "host workstation" are considered synonymous to each other. If this is a typing error, other interpretation could have been "test bench call back process", then appropriate corrections are required. Examiner is taking the second interpretation for claim prosecution.

8. Claim 34 is objected for the same reasons as claim 29 above.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

9. **Claims 1-11, 13-15, 17-30, 32-34 & 36 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 5,838,948 issued to Geoffrey J. Bunza (BU '948 hereafter).**

   Regarding Claim 1

   BU '948 teaches a behavior processor system for operating a portion of user design and interfacing it with the host test bench process (BU '948: Fig.5, 6; Col.10 Lines 60-65). BU '948 teaches a reprogrammable logic element (BU '948: Col.9 Lines 8-12) for modeling a hardware model for a portion of the user design that includes behavioral level functions (BU '948: Col.5 Lines 62-67; Col.6 Lines 10-13). Further,

BU '948 teaches a test bench call back process as control program and associated circuitry that surrounds the hardware emulation environment that communicates with the software simulator, simulating the other hardware control circuitry on the host test bench (BU '948: Col.13 Lines 55-60; Col.10 Lines 43-46, 60-65; Col.11 Lines 11-16). Further, BU '948 teaches the test bench call back process responding to the behavioral level function in the reprogrammable logic element by sending a signal to the host test bench process (BU '948: Fig. 7; Col.12 Lines 63-67; Col.13 Lines 1-6, 8-13).

Regarding Claim 2 & 3

BU '948 teaches that the behavioral level function includes a condition (BU '948: Col.13 Lines 55-64) and occurrence of these conditions triggers the test bench call back process (BU '948: Col.13 Lines 17-23).

Regarding Claim 5 & 6

BU '948 teaches the signal including an interrupt from the test bench call back process to the host test bench process as an I/O trap (BU '948: Col.13 Lines 8-36; 60-64), initiated by the reprogrammable logic element (as processor emulator).

Regarding Claim 7

BU '948 teaches that signal going from the test bench call back process to host test bench process includes data (BU '948:Col.12 Lines 25-32; 4-6).

Regarding Claim 8

BU '948 teaches that reprogrammable logic element temporarily suspends operation upon the occurrence of a condition (BU '948: Col.15 Lines 8-13).

Regarding Claim 9

BU '948 teaches that reprogrammable logic resumes operation from the point at which operation was temporarily suspended upon service of the signal by the host test bench (BU '948: Col.15 Lines 8-35).

Regarding Claim 10

BU '948 teaches that reprogrammable logic element temporarily pauses operation on occurrence of a condition (BU '948: Col.7 Lines 63-67; Col.15 Lines 8-13).

Regarding Claim 11

BU '948 teaches reprogrammable logic element includes a clock that controls the speed of processing instructions and data in reprogrammable logic element (BU '948: Col.7 Lines 61-67).

Regarding Claim 13

Claim 13 discloses the similar limitations as claim 1 is rejected for the same reasons as claim 1. BU '948 teaches Behavioral processor as software kernel, control program and associate control circuitry surrounding the hardware emulator (BU '948: Col.13 Lines 55-60).

Regarding Claim 14

BU '948 teaches modeling a hardware model for a portion of the user design that includes behavioral aspects of the user design (BU '948: Col.5 Lines 62-67; Col.6 Lines 10-13).

Regarding Claim 15

Claim 15 discloses the similar limitations as claim 2 is rejected for the same reasons as claim 2.

Regarding Claim 17

Claim 17 discloses the similar limitations as claim 1 is rejected for the same reasons as claim 1.

Regarding Claim 18

Claim 18 discloses the similar limitations as claim 3 is rejected for the same reasons as claim 3.

Regarding Claim 19

Claim 19 discloses the similar limitations as claim 8 is rejected for the same reasons as claim 8.

Regarding Claim 20

Claim 20 discloses the similar limitations as claim 9 is rejected for the same reasons as claim 9.

Regarding Claim 21

Claim 21 discloses the similar limitations as claim 10 is rejected for the same reasons as claim 10.

Regarding Claim 22

Claim 22 discloses the similar limitations as claim 8 is rejected for the same reasons as claim 8. Further, BU '948 teaches wait is executed by the reprogrammable logic element (BU '948: Col.7 Lines 63-67) on occurrence of a condition.

Regarding Claim 23

Claim 23 discloses the similar limitations as claim 9 is rejected for the same reasons as claim 9.

Regarding Claim 24

Claim 24 discloses the similar limitations as claim 10 is rejected for the same reasons as claim 10.

Regarding Claim 25

BU '948 teaches behavior processor operates when it receives request for service from the host workstation as target circuitry software simulation model running on the host workstation, generating an interrupt for service from processor emulator (BU '948: Col.12 Lines 19-26).

Regarding Claim 26

BU '948 teaches behavior processor operates when it receives request for service from the reprogrammable logic element as interrupt from the processor emulator (target microprocessor) (BU '948: Col.12 Lines 4-19).

Regarding Claim 27

Claim 27 discloses the similar limitations as claim 1 is rejected for the same reasons as claim 1.

Regarding Claim 28

Claim 28 discloses the similar limitations as claim 9 is rejected for the same reasons as claim 9.

Regarding Claim 29

BU '948 teaches suspending operation until the test bench call back process services the signal (BU '948: Col.15 Lines 8-13).

Regarding Claim 30

Claim 30 discloses the similar limitations as claim 2 is rejected for the same reasons as claim 2.

Regarding Claim 32

Method claim 32 discloses the similar limitations as claim 1 is rejected for the same reasons as claim 1. Further, BU '948 teaches the sending of an interrupt from the test bench call back process to the host/test bench process as an I/O trap (BU '948: Col.13 Lines 8-36; 60-64), initiated by the reprogrammable logic element (as processor emulator).

Regarding Claim 33

Claim 33 discloses the similar limitations as claim 9 is rejected for the same reasons as claim 9.

Regarding Claim 34

BU '948 teaches suspending operation until the test bench call back process services the signal (BU '948: Col.15 Lines 8-13).

Regarding Claim 36

Claim 36 discloses the similar limitations as claim 11 is rejected for the same reasons as claim 11.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 4,16,31 & 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,838,948 issued to Geoffrey J. Bunza (BU '948 hereafter), in view of IEEE Std 1364-1995 "IEEE Standard Hardware Description Language Based n the Verilog Hardware Description Language" (IEEE 1364 hereafter).

Regarding Claim 4

BU '948 teachings are disclosed in the claim 2 and the preceding claim 1 rejection above.

BU '948 does not teach that condition includes "if-then" conditional statement implemented in hardware.

IEEE 1364 teaches behavioral state machine model in which the states can be written in "if-then" conditional format (IEEE 1364: Example 2 showing the "if-then" scenario with op-code processing in an ALU/processor). The processor on the most generic form is a state machine.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply teachings of **IEEE 1364** to **BU '948** to include an "if-then" conditional statement in the behavioral level function on the reprogrammable logic element. The motivation would have been that the hardware model for the reprogrammable logic element is designed using the hardware description language's like VHDL (BU '948: Col.5 Lines 50-53) and IEEE 1364 teaches Verilog as an industry standard for HDL based design (IEEE 1364: Introduction).

Regarding Claim 16

Claim 16 discloses the similar limitations as claim 4 is rejected for the same reasons as claim 4.

Regarding Claim 31

Claim 31 discloses the similar limitations as claim 4 is rejected for the same reasons as claim 4.

Regarding Claim 35

Claim 35 discloses the similar limitations as claim 4 is rejected for the same reasons as claim 4.

11. **Claims 12 & 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,838,948 issued to Geoffrey J. Bunza (BU '948 hereafter), in view of IEEE article "A 145MHz User-Programmable Gate Array" by Eduardo do Valle Simoes et al (ED 1995 hereafter).**

Regarding Claim 12

BU '948 teachings are disclosed in the claim 11 and the preceding claim 1 rejection above.

BU '948 does not teach reprogrammable logic element clock running at 20 MHz.

ED 1995 teaches reprogrammable logic element clock running at frequency of 145 MHz (ED 1995: Pg.226 Col.2 Section 1.1 Lines 8-10).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply teachings of **ED 1995** to **BU '948** and make the reprogrammable logic element run at any frequency up to 145 MHz. The motivation would have been that **ED 1995** teaches the fast implementation using FPGA matrix (ED 1995: Abstract) using strategy to place logic cell in row. Hence it would have been easy to run the implantation at a lower speeds using XILINX XC300 Family FPGA as well (ED 1995: Pg.232 Col.1 Lines 1-3).

Regarding Claim 37

Claim 37 discloses the similar limitations as claim 12 is rejected for the same reasons as claim 12.

Conclusion

12. The prior art made of record and not relied upon in PTO 892 is considered pertinent to applicant's disclosure.

13. All claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 8:30 - 5:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R. Homere can be reached on (571)272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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